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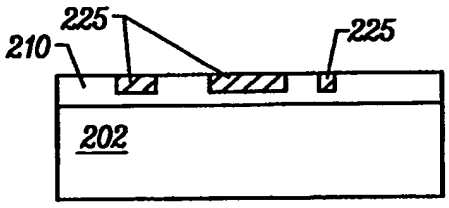
(54) Title: ENDPOINT DETECTION METHOD FOR CMP PROCESSES

(57) Abstract

A method is disclosed that determines an endpoint to a CMP process by monitoring the surface topography (225) of the semiconductor wafer (202) being polished. When it is determined that the wafer surface has a substantially unpatterned appearance, appearing to look like a blank wafer, an endpoint to the polishing process is indicated and the CMP process stops thereafter. The method is ideal for use when polishing opaque materials where layer thickness is impractical to be measured.



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ENDPOINT DETECTION METHOD FOR CMP PROCESSES

BACKGROUND OF THE INVENTION

Field of Invention

The invention relates to a method for detecting an endpoint in chemical-mechanical polishing of semiconductor wafers.

Background

In the production of semiconductor devices, chemical-mechanical polishing (CMP) is used to remove material from the semiconductor wafer surface to smooth the wafer surface. Generally, in CMP processes, a semiconductor wafer is rubbed against an abrasive polishing pad with a controlled amount of pressure in the presence of a chemically reactive slurry. The slurry generally contains small, abrasive particles that abrade the surface of the wafer and chemicals that etch and/or oxidize the surface of the wafer. When the pad and the wafer are moved with respect to one another, material is removed from the surface of the wafer by abrasive particles in the pad and in the slurry (mechanical removal) and by the chemicals (chemical removal) in the slurry.

Fig. 1 shows a generic cross-sectional representation of a CMP machine 100. The machine includes the platen 110 on which is placed an abrasive pad 115. A slurry 120 is introduced onto the surface of the abrasive pad 115 by a slurry dispenser 125. Semiconductor wafer 130 is secured to carrier arm 135 so that the surface of the semiconductor wafer 130 when lowered will come into contact with slurry 120 and polishing pad 115. The platen 110 and the carrier arm 135 can each be rotated in the same direction as indicated by lines 140 and 142, can be rotated in opposing directions, or can be actuated in a back and forth manner as indicated by line 144. When the wafer surface is brought into contact with the polishing pad 115 and slurry 120 by the carrier arm 135, the carrier arm and the platen 110 are moved relative to one another such that the polishing pad 115 and slurry 120 remove surface material from the wafer 130.

It is important that a CMP process accurately stop polishing a wafer at a particular desired endpoint. For instance, in damascene processes, trenches are formed in an insulating layer, and conductive material is made to fill the trenches. Usually, when formed, the conductive layer not only fills the trenches, but extends above the trenches as well and must be polished down. When the conductive layer is being polished, if underpolishing occurs, or not enough of the surface material is removed, conductive material will remain above the trenches, creating shorts in the semiconductor wafer. If, however, the surface is overpolished, other

problems can result such as portions of the structure breaking, or removal of too much of the conductive layer causing lack of a conductor in a desired area.

Many methods have been developed in determining CMP endpoints, for instance, measuring of load current and measuring layer thickness. Nonetheless, these methods are not particularly effective when polishing a conductive metal layer such as aluminum and/or copper. For instance, when measuring load current to determine when the endpoint has been reached, a load to the spindle of the carrier arm will vary according to frictional forces. Thus when metal above trenches has been polished away, the frictional load will cause a change in the motor current. Such a method works well when the metal areas to be filled are for vias since vias are small compared to the rest of the insulator surface. However, when large trenches are to be filled with metal, a strong signal indicating a change in drive current will not be obtained.

Measuring layer thickness is also not very useful for detecting an endpoint when polishing a metal, or other opaque, layer. Such a technique is most useful when the layer being removed is an insulating layer, typically an oxide, which is transparent. To measure layer thickness, images of the wafer surface are taken while the insulating layer is being removed. Such images can be taken either by oscillating the wafer off the platen where the slurry is rinsed and an image taken, or by embedding sensors in the polishing pad. The images are inspected and the thickness of the insulating layer is determined. Because insulating layers such as oxide layers are transparent, determining the insulating layer thickness is relatively easy using optical reflectometry. However, such a method will not be useful for opaque metals such as aluminum and copper.

Thus, it is desirable to develop an endpoint detection process that can be used for endpoint detection with opaque layers, such as metal layers.

SUMMARY OF THE INVENTION

In order to overcome the deficiencies described above with respect to CMP endpoint detection, particularly when polishing opaque layers, a method in accordance with the invention is disclosed. Generally described, a method in accordance with the invention monitors the surface appearance of a semiconductor wafer being polished. When the wafer surface appearance changes, an endpoint is signaled and polishing is stopped thereafter. In some embodiments of the invention, the wafer surface appearance will change from having a patterned surface to a substantially unpatterned surface. In other embodiments of the invention, the wafer surface appearance will change from having a substantially unpatterned surface to one having a patterned surface. The wafer surface appearance is optically monitored by a human eye in some embodiments, while other embodiments utilize a machine to monitor the wafer surface appearance.

A method in accordance with the invention will reduce uncertainty in the CMP stopping point over conventional processes, particularly for opaque materials. Moreover, such a process will be relatively inexpensive to implement.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described with respect to particular embodiments thereof, and reference will be made to the drawings, which are not necessarily drawn to scale, and in which:

Fig. 1 is a cross-sectional view of conventional chemical-mechanical polishing apparatus;

Fig. 2 is a three-dimensional, cross-sectional view of a patterned insulating layer formed on a semiconductor wafer;

Fig. 3 is a flat cross-sectional view of the insulating layer of Fig. 2 further having a barrier layer and a metal layer formed thereon;

Fig. 4 is the cross-sectional view of the structure shown in Fig. 3 after having been polished;

Fig. 5 is the cross-sectional view of the structure shown in Fig. 3 immediately prior to completing the CMP in accordance with the invention;

Fig. 6 is a generalized overhead view of a semiconductor wafer having a raised topography;

Fig. 7 is an overhead view of the wafer of Fig. 6 immediately prior to completing the CMP in accordance with the invention; and

Fig. 8, including Figs. 8a-8e, illustrate steps in accordance with one embodiment of the invention; and

Fig. 9 is a cross-sectional view of a dielectric layer etched with narrow trenches for forming contacts; and

Fig. 10 is a close-up, cross-sectional view of the structure of Fig. 4 and showing "dishing."

DETAILED DESCRIPTION

A method is provided for determining the endpoint in a CMP process where an opaque material is being polished. The method includes inspecting the wafer surface to determine if the surface appearance has changed, e.g., from a patterned surface to a substantially unpatterned surface, and vice versa. Upon confirmation of a change in appearance, an endpoint to the polish process is indicated.

Referring to Fig. 2 a dielectric layer 210 has been etched with trenches 215 as shown, resulting in the layer 210 having varying elevations. Dielectric layer 210 can be formed of

oxide or other insulating materials as is known in the art. Such a dielectric layer 210 is typically formed over other layers of a semiconductor device, which are not shown. The other layers (not shown) can include insulating layers, metal layers, or active device layers. A metal, such as copper or aluminum, is to be deposited in each of the trenches 215 formed in dielectric layer 210.

As shown in Fig. 3, prior to forming metal layer 225, often a barrier layer 220 is grown or deposited over dielectric layer 210. Barrier layer 220 is useful to increase adhesion of the metal layer and/or improve contact resistance. When copper is to be used for metal layer 225, the barrier layer 220 is often formed of titanium nitride, titanium tungsten, tantalum, tantalum nitride, or other appropriate film as is known in the art. Metal layer 225 is then deposited over dielectric 210 and barrier layer 220, if used.

As shown, the metal layer 225 is conformal to the underlying dielectric layer 210 but is not planar. In other words, the metal layer 225 replicates to some extent the topographical structure of the dielectric layer 210 beneath, also having varying elevations. It is generally desirable to polish the semiconductor surface until the structure resembles that of Fig. 4, such that the surface is smooth and metal remains in trench regions 215 only.

Referring again to Fig. 3, when metal layer 225 is formed, the wafer surface will have a patterned appearance that is identifiable, often optically with the naked eye, when viewed from above resulting from the varying elevational topography. Fig. 6 illustrates a generalized example of how the wafer surface might appear when the wafer 600 is viewed from above. Similarly, when polishing is finished, metal regions will be distinguishable, often visually, from dielectric regions on the wafer surface. However, when polishing the metal layer 225, a point will be reached immediately prior to complete removal of the undesirable portions of the metal layer when the wafer surface will have a distinct appearance from that demonstrated in Figs. 3, 4, and 6. This visually distinct appearance of the wafer is shown in Figs. 5 and 7. As shown in Fig. 5, the surface of the metal layer 225 will be substantially smooth and as shown in Fig. 7, when viewed from above the wafer will appear to look like a blank wafer having nothing developed upon it. The surface of the wafer will have few, if any, identifiable pattern marks.

This point where the wafer has an unpatterned, or blank wafer-like, appearance is used in accordance with the invention to mark an endpoint for the CMP process. When this endpoint is detected, only a thin layer of metal 225 above the dielectric layer needs to be polished off, as shown in Fig. 5. This thin layer can be removed in a matter of seconds, depending upon the slurry used and the abrasive rate of the polishing pad. In one embodiment of the invention the slurry will remove a copper layer at an average rate of approximately 2000 Å per minute,

causing only a few seconds of polishing to be necessary once the ndpoint is detected. In other embodiments, the slurry may remove the metal layer at a faster or slower rate.

In one embodiment of the invention, an unpatterned, or blank-wafer-like, appearance can be determined with a naked human eye. In other embodiments, defect metrology using defect inspection tools such as those manufactured by KLA (e.g., KLA 2135) or Inspex (e.g., Inspex TPC85), as are known in the art, can be used to detect the endpoint described above. Defect metrology is used, as is known in the art, to register a pattern and/or to detect any deviation in a pattern on a wafer. Therefore, a defect metrology system is utilized in one embodiment of the invention to monitor the surface of the wafer during polishing. For instance, when the defect metrology system detects a change from a patterned appearance to a substantially unpatterned appearance on the wafer surface, the system can trigger a signal that serves as an endpoint signal. In using defect metrology, sensors could be placed under the polishing pad in some embodiments of the invention, or the wafer could be oscillated off of the platen and an image taken for comparison by a computer to other images of unpatterned surfaces in other embodiments. Still other embodiments of the invention may utilize other methods known in the art of monitoring the surface pattern appearance.

Once a blank-wafer-like appearance is detected, then depending on the polishing pad, the polish rate, and the metal being polished, the additional time to remove the rest of the layer can be determined and optimized. Thus, using an endpoint detection method in accordance with the invention, a much smaller uncertainty in the CMP stopping point can be achieved than when using some conventional processes.

In some embodiments of the invention, which utilize a barrier layer 220, two polishing steps may be used: one for the metal layer 225 and a second, which polishes at a different rate than the first, for the barrier layer 220. In such a case, once a blank-wafer-like appearance is detected, the polish of the metal layer can continue for a short time as discussed above. Then a second polish at a different rate can be used to finish removing portions of the barrier layer 220. Such a second polish will also take only a short time as the barrier layer is typically 100-300 Å.

Fig. 8 shows the steps as used in a method in accordance with the invention. A semiconductor wafer 202 is provided, which generally includes a substrate and may also include active device layers, insulating layers, and/or conducting layers. A dielectric layer 210 is formed on semiconductor wafer 202 by growth or deposition, resulting in the structure shown in Fig. 8a. The dielectric layer 210 is then etched as is generally known in the art, to form trenches 215, which may have varying widths. The resulting structure is shown in Fig. 8b. A metal layer 225 is formed over the patterned surface of the dielectric layer 210. The metal will conform to the pattern etched in the dielectric layer 210 as shown in Fig. 8c. Optionally, in

some embodiments, a barrier layer may be formed on the patterned dielectric layer 210 prior to forming the metal layer 225, as discussed previously. The metal layer 225 is then polished using a CMP process and apparatus as described with respect to Fig. 1. With reference to Fig. 8d, an endpoint is determined when a blank-wafer-like appearance is detected, i.e., when only a smooth metal layer without pattern is observed. Polishing of the wafer surface stops shortly thereafter to result in Fig. 8e.

In alternative embodiments of the invention, the process as described with respect to Fig. 8 may be performed in a somewhat reverse manner. In other words, rather than starting with a patterned surface and detecting an unpatterned surface as an endpoint, an alternative embodiment of the invention will start with a substantially unpatterned surface and detect a patterned surface as the endpoint. For instance, referring to Fig. 9, when dielectric layer 910 is etched only with narrow trenches, e.g., for forming contacts, when metal layer 925 is deposited, the metal layer may initially appear substantially like a blank wafer, with little to no pattern visible. Once polished sufficiently, however, a pattern on the wafer surface will be visible, indicating an endpoint to the polish process.

Thus, a method in accordance with the invention has been described which monitors the wafer surface for changes in appearance. Such changes can be from a patterned surface to a substantially unpatterned surface and vice versa. Some embodiments of the invention may even monitor for changes in pattern, i.e., monitor for a change from a first patterned surface to a second patterned surface. Once a particular change in surface appearance is detected, an endpoint to the CMP process is indicated.

Using a method in accordance with the invention has resulted in good "dishing" in the semiconductor wafer. Referring to Fig. 10, "dishing" is an indentation in the surface of the metal regions formed in trenches 215. The "dishing" phenomena occurs because often the metal will be polished at a faster rate than the dielectric. A small amount of "dishing", as obtained when using a method in accordance with the invention, indicates that the CMP process has been stopped at an appropriate point. If the CMP process were to continue, "dishing" would become much more pronounced -- an undesirable effect.

It should be understood that the particular embodiments described above are only illustrative of the principles of the present invention, and various modifications could be made by those skilled in the art without departing from the scope and spirit of the invention. For instance, such a process could be used with the CMP of any opaque layer, and the invention should not be construed as being limited to the CMP of copper, aluminum, or metals in general. Thus, the scope of the present invention is limited only by the claims that follow.

CLAIMS

What is claimed is:

1. A method of fabricating a semiconductor integrated circuit, comprising the steps of:

(a) polishing a semiconductor wafer (202) using a CMP process wherein said semiconductor wafer has a surface appearance (210, 215, 225); and

(b) detecting a CMP process endpoint by detecting a change in said surface appearance.

2. The method of claim 1, further including the step of stopping the step of polishing subsequent to said step (b).

3. The method of claim 1, wherein step (b) includes detecting said change when said surface appearance has changed from a patterned appearance to a substantially unpatterned appearance.

4. The method of claim 1, wherein step (b) includes detecting said change when said surface appearance has changed from a substantially unpatterned appearance to a patterned appearance.

5. The method of claim 1, wherein said step (b) is carried out using a defect metrology process.

6. A method of fabricating a semiconductor integrated circuit on a semiconductor wafer (202) having a layer (210) formed thereon said layer having varying elevations (215), comprising the steps of:

(a) forming a conformal layer (225) over said layer having varying elevations;

(b) polishing said conformal layer using a CMP process; and

(c) monitoring for a CMP process endpoint by comparing a surface appearance of said semiconductor wafer to an endpoint surface appearance.

7. The method of claim 6, wherein in step (c), said endpoint surface appearance is a substantially blank-wafer-like appearance.

8. The method of claim 6, wherein said conformal layer is opaque.

9. The method of claim 8, wherein said having said conformal layer is a conformal metal layer.

10. The method of claim 6, wherein said step (c) includes optically viewing the surface of said semiconductor wafer.

11. The method of claim 10, wherein said step of optically viewing is performed by a machine, wherein said machine takes an image of said wafer and compares said image to a stored image.

12. A method of fabricating an integrated circuit on a semiconductor wafer (202), comprising the steps of:

(a) forming, over said semiconductor wafer, a dielectric layer (210) having trenches (215) formed therein;

(b) forming a conformal metal layer (225) over said dielectric layer such that the metal layer fills said trenches and forms a patterned surface appearance on said semiconductor wafer;

(c) performing a CMP process on said semiconductor wafer;

(d) stopping said CMP process after detection of a substantially unpatterned surface appearance on said semiconductor wafer.

13. A method of fabricating an integrated circuit on a semiconductor wafer (202), comprising the steps of:

(a) forming, over said semiconductor wafer, a dielectric layer (210), having trenches (215) formed therein;

(b) forming a conformal metal layer (225) over said dielectric layer such that the metal layer fills said trenches and forms a substantially unpatterned surface appearance on said semiconductor wafer;

(c) performing a CMP process on said semiconductor wafer; and

(d) stopping said CMP process after detection of a patterned surface appearance on said semiconductor wafer.

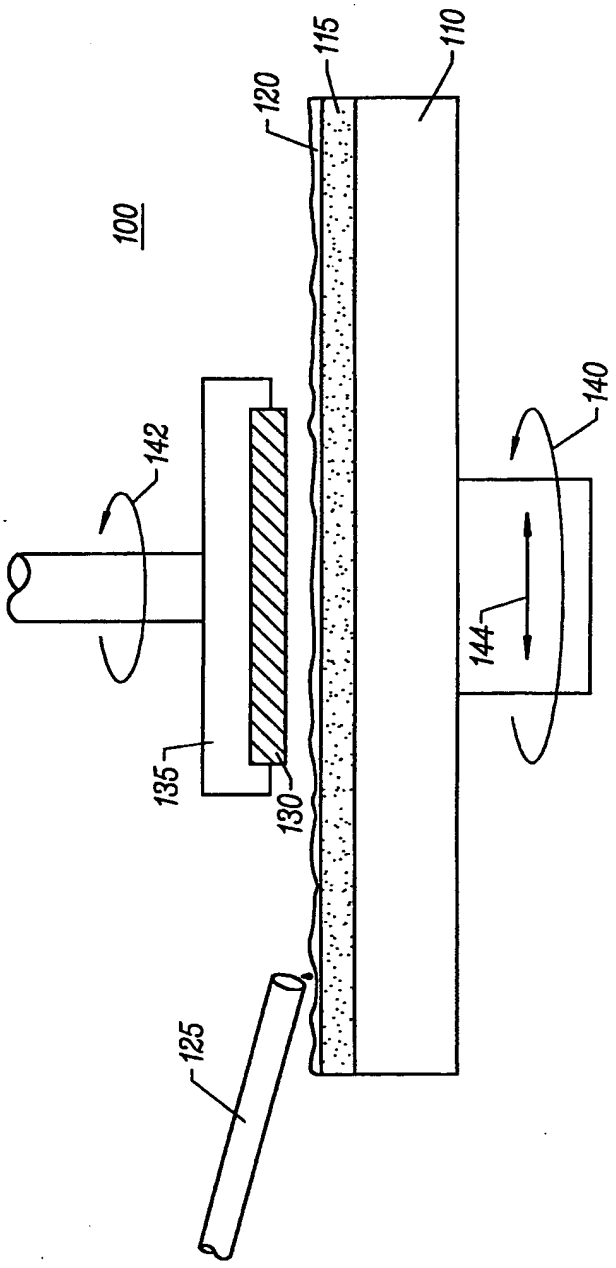

FIG. 1

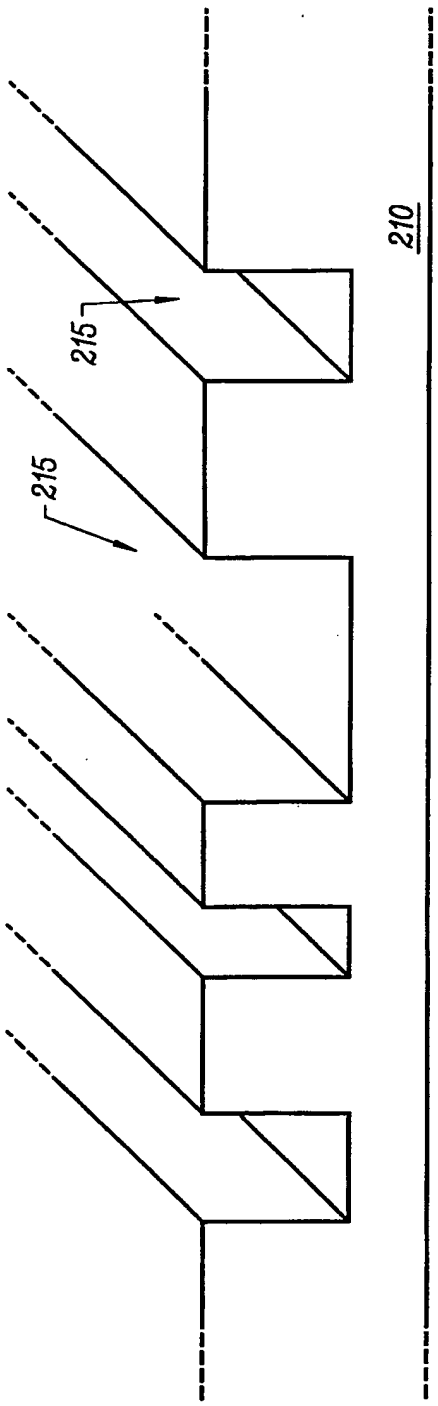

FIG. 2

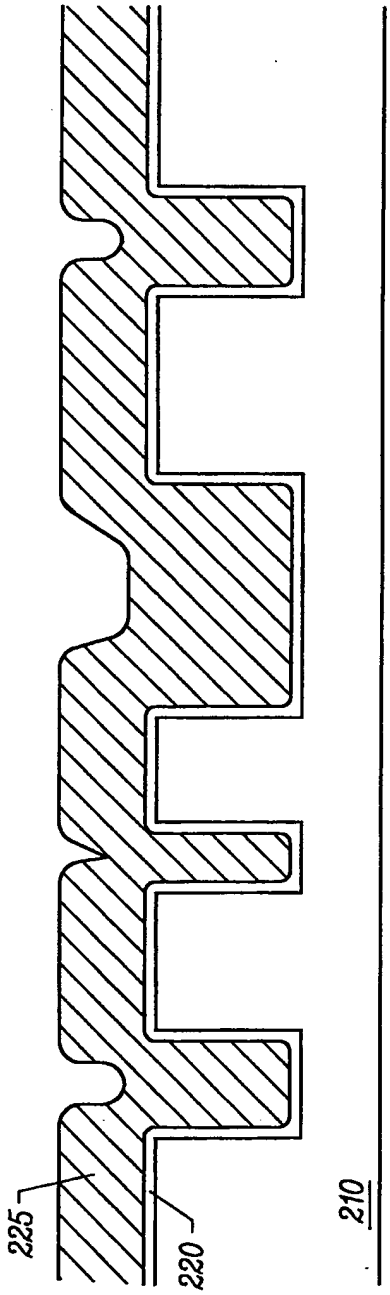

FIG. 3

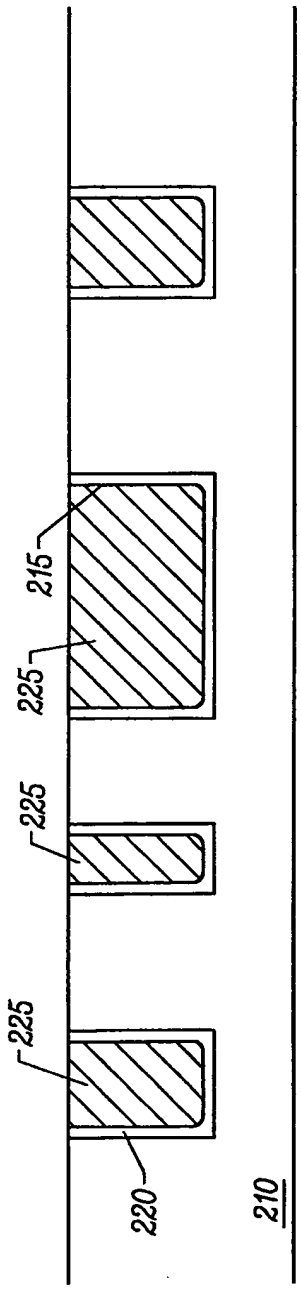

FIG. 4

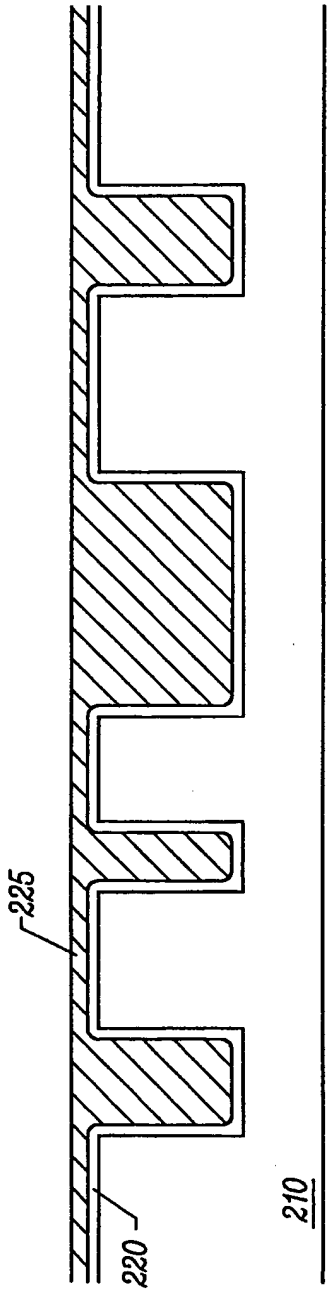

FIG. 5

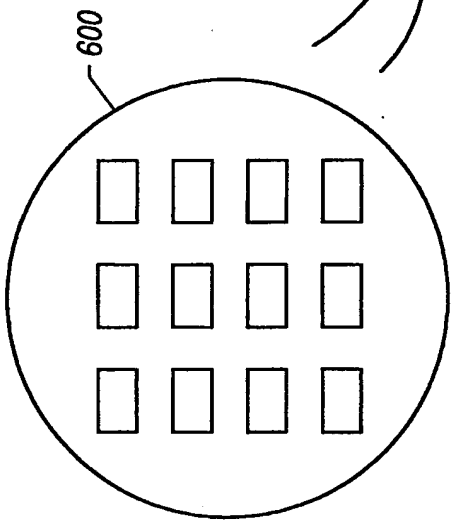

FIG. 6

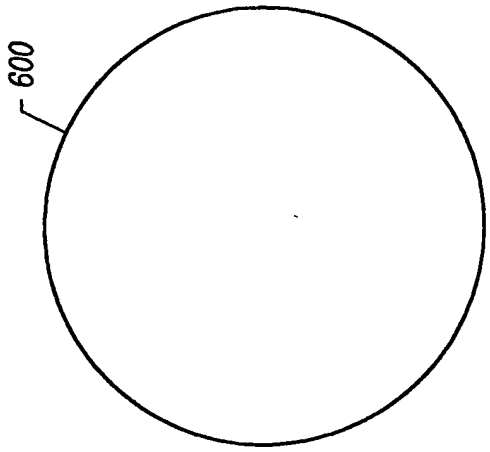

FIG. 7

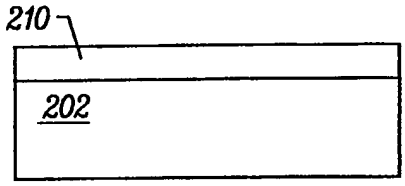

FIG. 8A

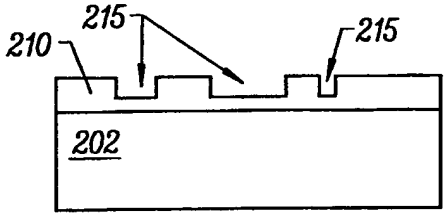

FIG. 8B

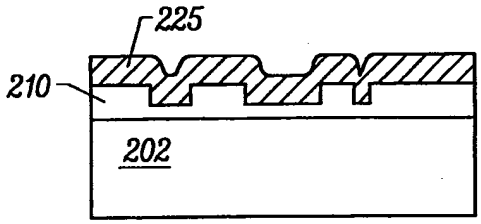

FIG. 8C

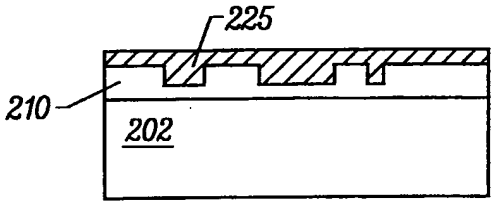

FIG. 8D

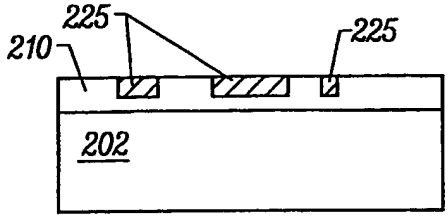

FIG. 8E

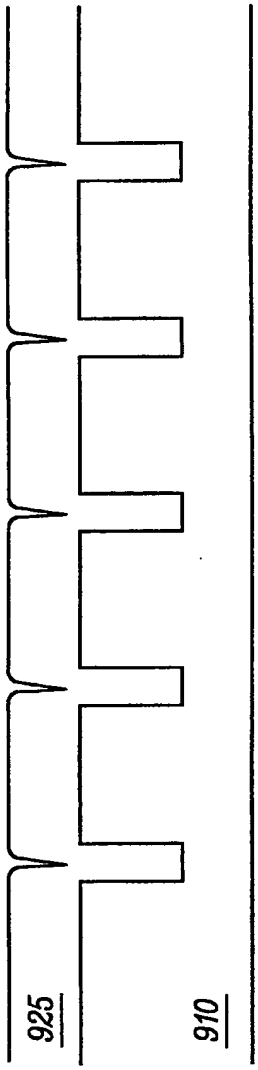

FIG. 9

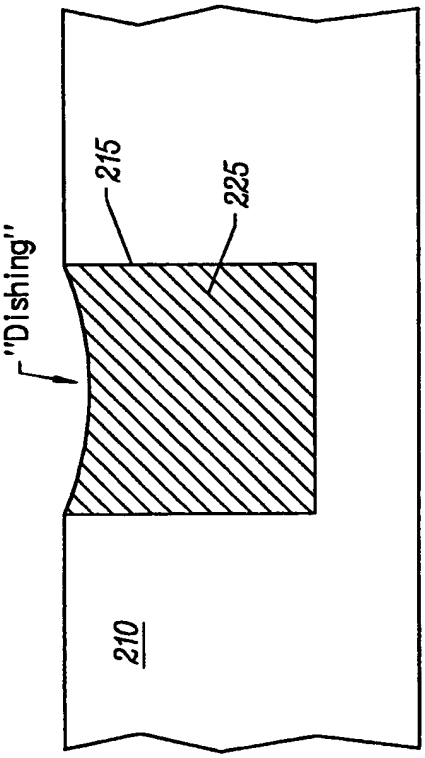

FIG. 10

INTERNATIONAL SEARCH REPORT

Inter nal Application No
PCT/US 98/25938

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G01B21/08 G01B11/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G01B H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 5 169 491 A (T.T. DOAN) 8 December 1992 see the whole document; see figures 1-4	1,2,6,7 8-13
X	EP 0 352 740 A (APPLIED MATERIALS INC.) 31 January 1990 see the whole document; see figures 1-6	1,2,4
X	PATENT ABSTRACTS OF JAPAN vol. 97, no. 3, 31 March 1997 & JP 08 292012 A (NEC CORP.), 5 November 1996 see abstract	1,2,5

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inter nal Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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